In the claims:

Please cancel claims 1-20 without prejudice.

Please add the following new claims:

21. (New) A method comprising:

generating a first test program to test the functionality of an integrated circuit (IC);

executing the first test program;

determining whether the IC has been sufficiently tested; and

if not, determining whether a predetermined test program population threshold has been reached.

22. (New) The method of claim 21, further comprising:

generating a second test program if the predetermined test program population threshold has been reached; and

executing the second test program.

23. (New) The method of claim 22, wherein generating the first test program comprises:

generating a first abstract syntax tree (AST);

generating a first set of instructions and data for the first AST; and

translating the first AST into a first executable test program.

24. (New) The method of claim 23, wherein generating the second test program comprises:

generating a second abstract syntax tree (AST);

generating a second set of instructions and data for the second AST; and

translating the second AST into a second executable test program.

25. (New) The method of claim 24, further comprising mutating a selected AST.

26. (New) The method of claim 25, wherein mutating a selected AST comprises:
selecting an AST;
removing a segment of the selected AST; and
inserting a replacement segment into the selected AST to form a mutated AST.

27. (New) The method of claim 26, further comprising:
generating a third set of instructions and data for the mutated AST; and
translating the mutated AST into a third executable test program.

28. (New) The method of claim 25, wherein mutating a selected AST comprises:
selecting the first AST and the second AST; and
combining a segment of the first AST with a segment of the second AST to form a mutated AST.

29. (New) The method of claim 28, further comprising:
generating a third set of instructions and data for the mutated AST; and
translating the mutated AST into a third executable test program.

30. (New) The method of claim 21, further comprising:
adding the first AST and corresponding coverage data into test program population after the first test program has been executed.

31. (New) A computer system comprising:
a storage device coupled to a processor and having stored therein at least one routine, which when executed by the processor, causes the processor to generate data, the routine causing the processor to,
generate a first test program to test the functionality of an integrated circuit (IC);

execute the first test program;

determine whether the IC has been sufficiently tested; and

determine whether a predetermined test program population threshold has been reached.

32. (New) The computer system of claim 31, wherein the routine further causes the processor to,

generate a second test program if the predetermined test program population threshold has been reached; and

execute the second test program.

33. (New) The computer system of claim 32, wherein generating the first test program comprises:

generating a first abstract syntax tree (AST);

generating a first set of instructions and data for the first AST; and

translating the first AST into a first executable test program.

34. (New) The computer system of claim 33, wherein generating the second test program comprises:

generating a second abstract syntax tree (AST);

generating a second set of instructions and data for the second AST; and

translating the second AST into a second executable test program.

35. (New) The computer system of claim 34, wherein the routine further causes the processor to mutate a selected AST.

36. (New) The computer system of claim 35, wherein mutating a selected AST comprises:

selecting an AST;

removing a segment of the selected AST; and

inserting a replacement segment into the selected AST to form a mutated AST.

37. (New) The computer system of claim 36, wherein the routine further causes the processor to,

generate a third set of instructions and data for the mutated AST; and

translate the mutated AST into a third executable test program.

38. (New) The computer system of claim 35, wherein mutating a selected AST comprises:

selecting the first AST and the second AST; and

combining a segment of the first AST with a segment of the second AST to form a mutated AST.

39. (New) The computer system of claim 38, wherein the routine further causes the processor to,

generating a third set of instructions and data for the mutated AST; and

translating the mutated AST into a third executable test program.

40. (New) The computer system of claim 31, wherein the routine further causes the processor to,

adding the first AST and corresponding coverage data into test program population after the first test program has been executed.

41. (New) A validation test system comprising:

a test builder to generate test programs to test the functionality of an integrated circuit (IC);

a test generator to translate the test programs into an executable test;

a test analyzer to execute the test programs; and

a feedback engine to build a test population of test programs by generating an abstract syntax tree (AST) for each test program.

42. (New) The system of claim 41, wherein the feedback engine determines whether a predetermined test program population threshold has been reached after a test program has been executed.

43. (New) The system of claim 42, wherein the feedback engine generates one or more mutated ASTs if it is determined that the predetermined test program population threshold has been reached.

44. (New) The system of claim 43, wherein the feedback engine generates a mutated AST by selecting a first AST, removing a segment of the first AST and inserting a replacement segment into the first AST.

45. (New) The system of claim 43, wherein the feedback engine generates a mutated AST by selecting a first AST and a second AST and combining a segment of the first AST with a segment of the second AST to form.